SpiNNaker
Biologically Inspired Massively Parallel Architectures

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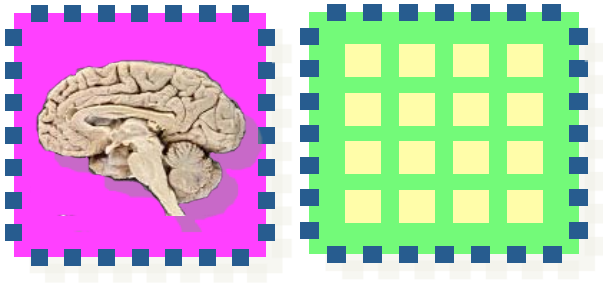

Programming a Million-Core Machine

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Bio-inspiration

- How can massively parallel computing resources accelerate our understanding of brain function?
- How can our growing understanding of brain function point the way to more efficient parallel, fault-tolerant computation?

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Building brains

- Brains demonstrate
  - massive parallelism (10^{11} neurons)
  - massive connectivity (10^{15} synapses)
  - excellent power-efficiency
    - much better than today's microchips
  - low-performance components (~ 100 Hz)
  - low-speed communication (~ metres/sec)
  - adaptivity – tolerant of component failure
  - autonomous learning

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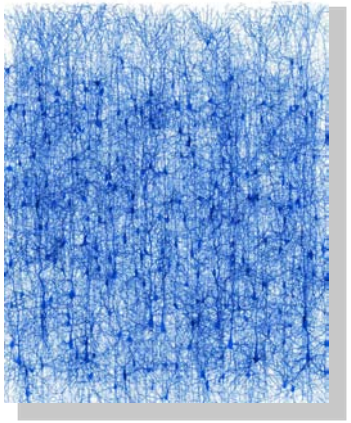
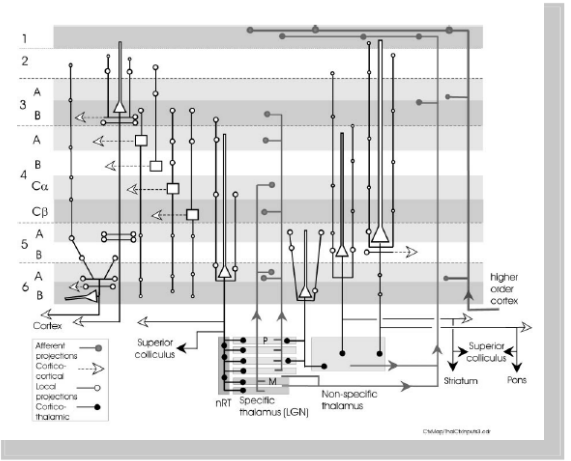
Building brains

- Neurons
  - multiple inputs, single output (c.f. logic gate)
  - useful across multiple scales (10^2 to 10^{11})
- Brain structure
  - regularity
  - e.g. 6-layer cortical 'microarchitecture'





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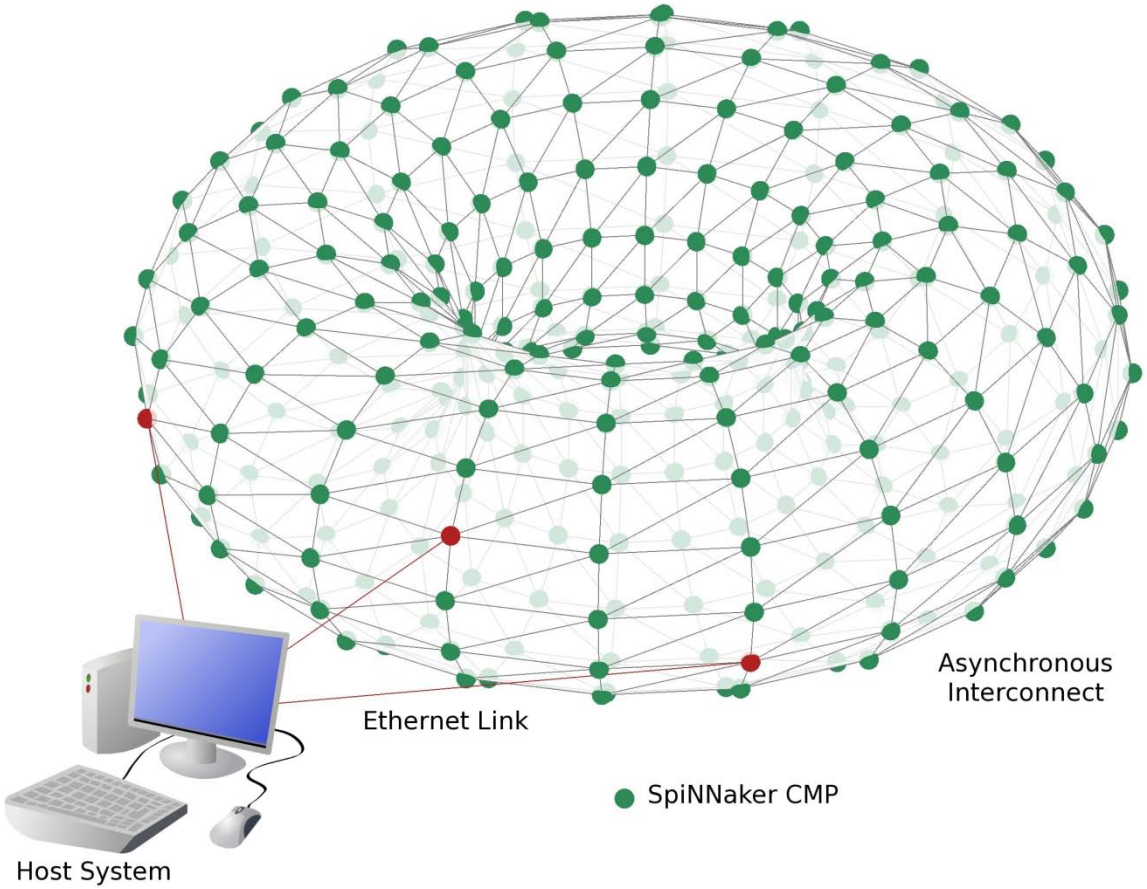
SpiNNaker project

- A million mobile phone processors in one computer
- Able to model about 1% of the human brain…
- …or 10 mice!



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Design principles

- *Virtualised topology*
  - physical and logical connectivity are decoupled
- *Bounded asynchrony*
  - time models itself
- *Energy frugality*
  - processors are free
  - the real cost of computation is energy

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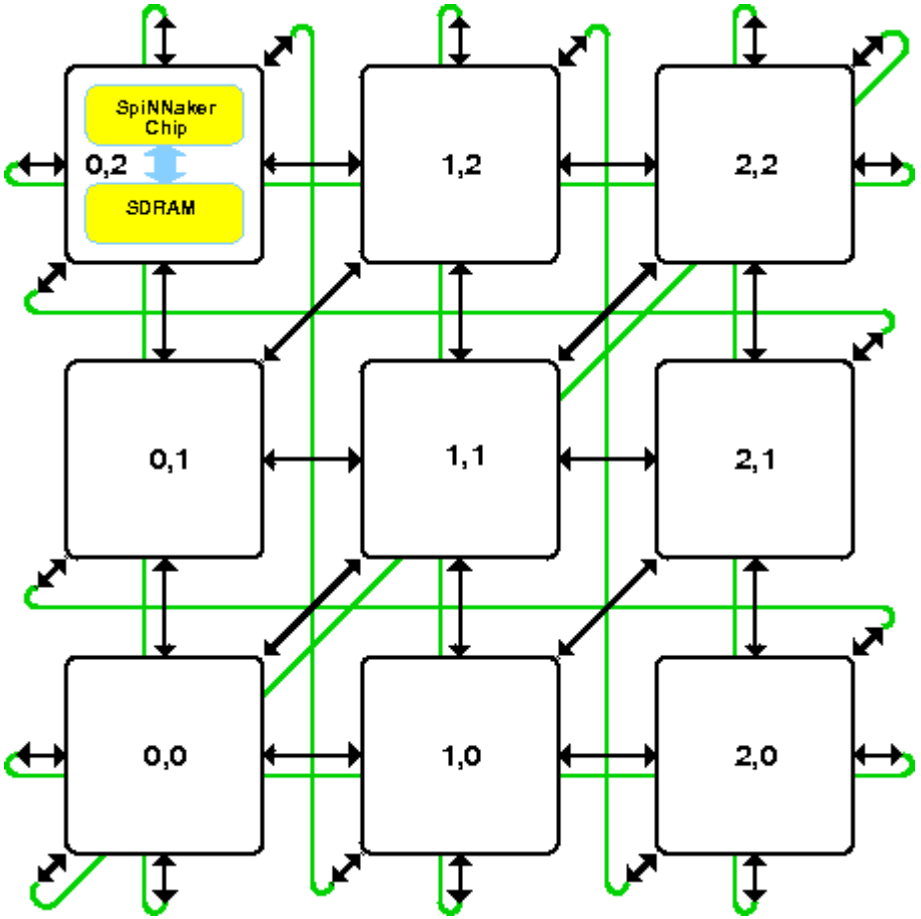
SpiNNaker system



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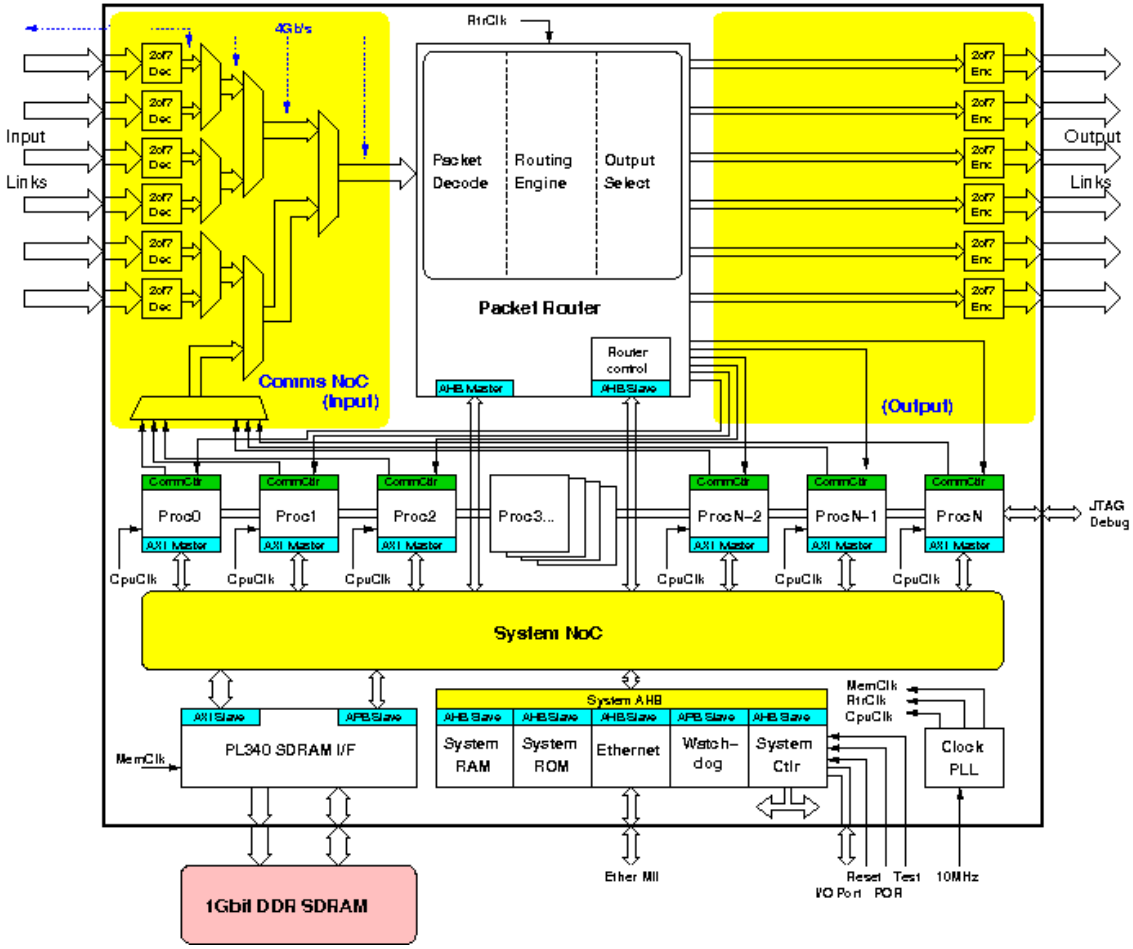
SpiNNaker node



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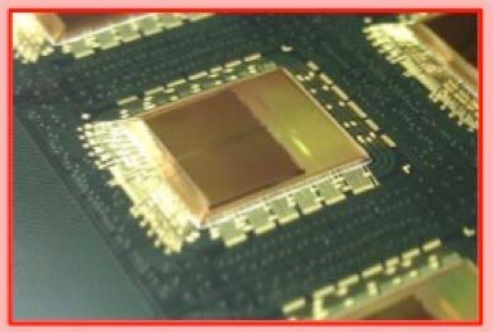
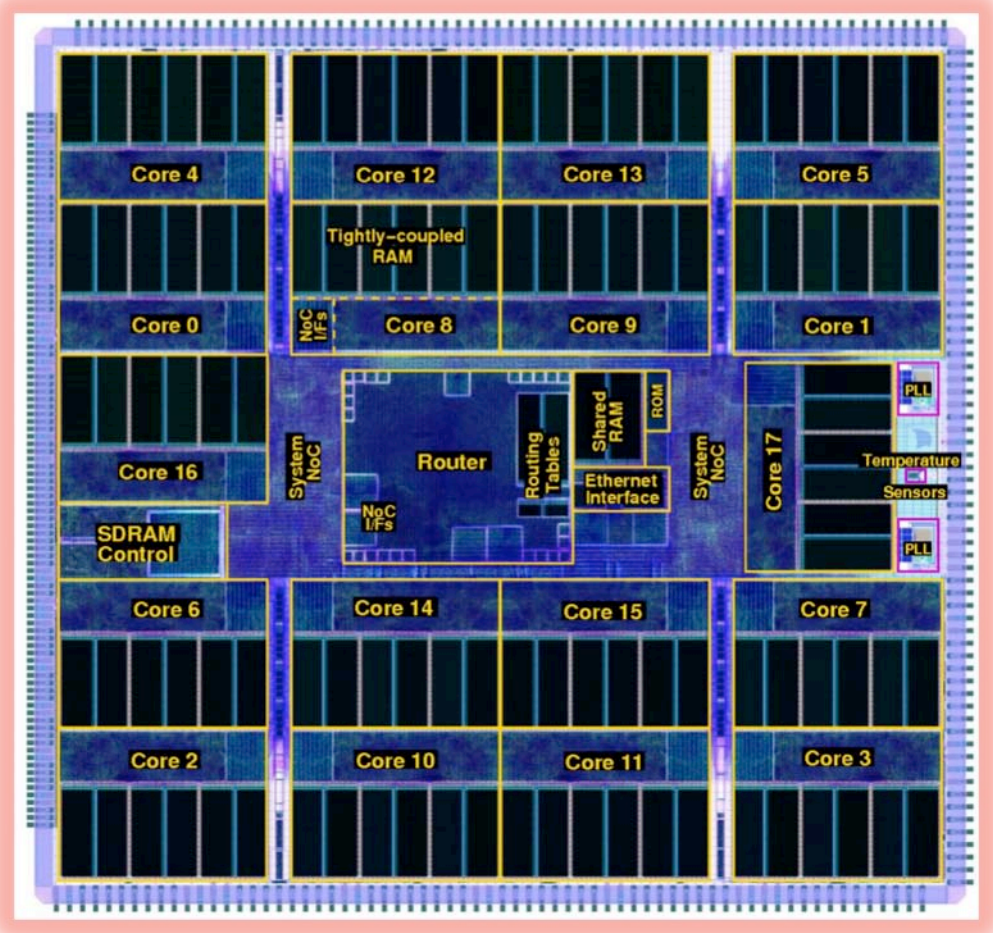
SpiNNaker chip



Mobile DDR SDRAM interface

Multi-chip packaging by UNISEM Europe



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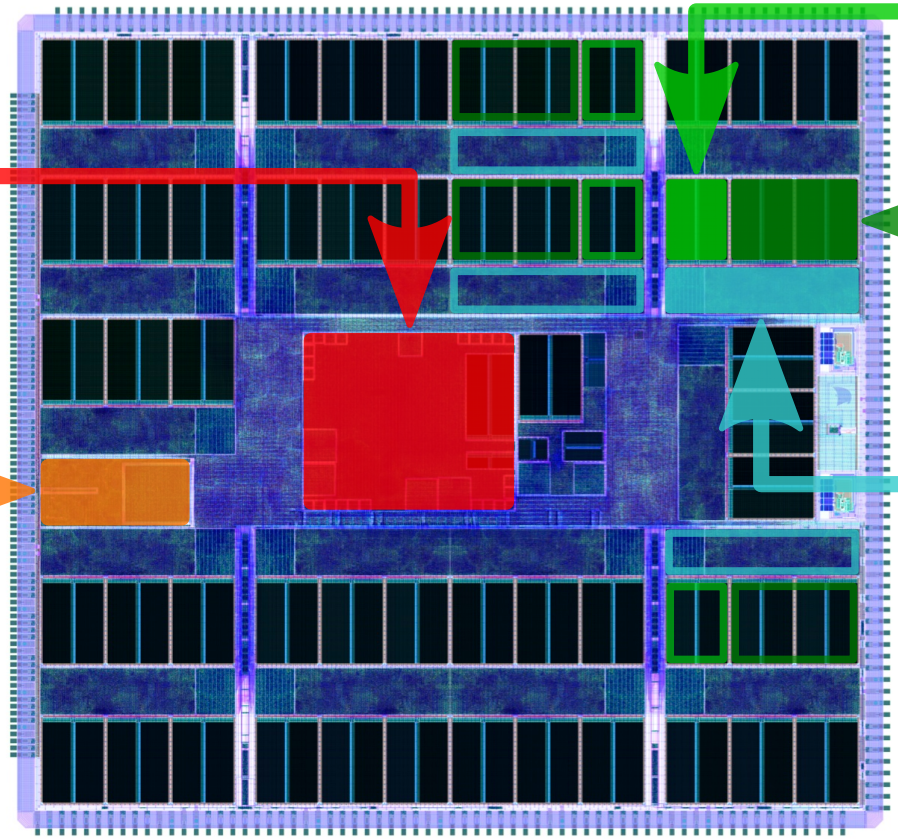
Chip resources



Instruction memory

run-time kernel
application callbacks

Data memory

kernel state
neuron states
stack and heap

Processor

neuron and synapse
state computations

Router

routing tables
spike packet routing
system comms.

RAM port

synapse states
activity logs

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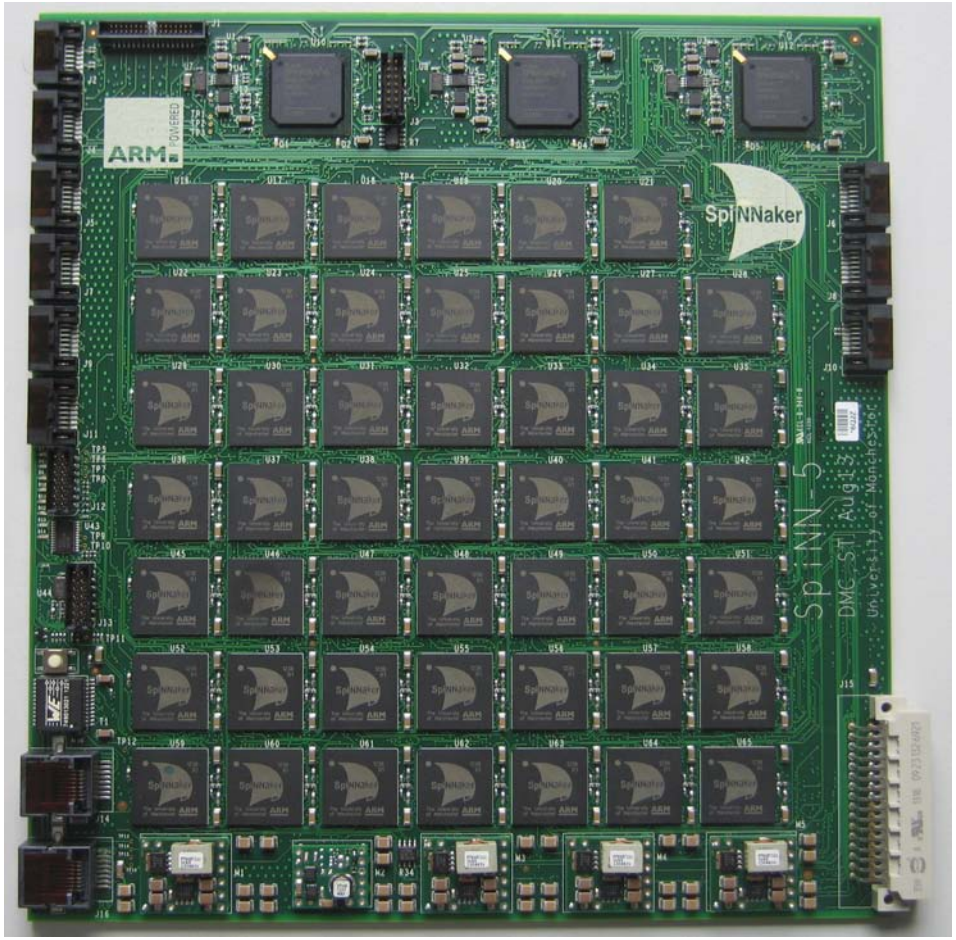
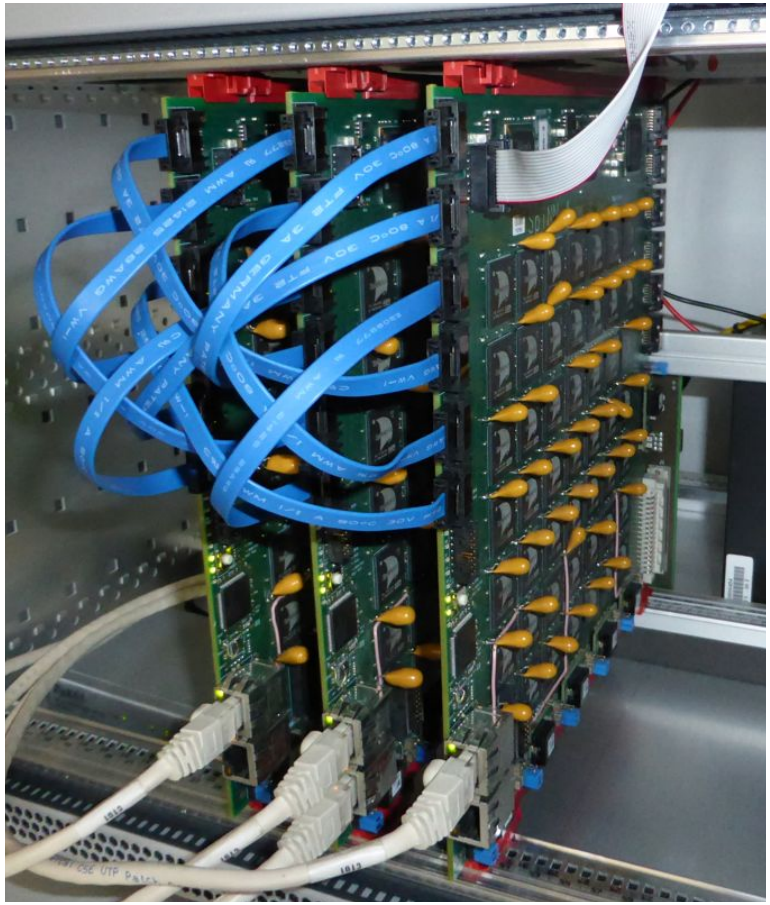
48-node PCB





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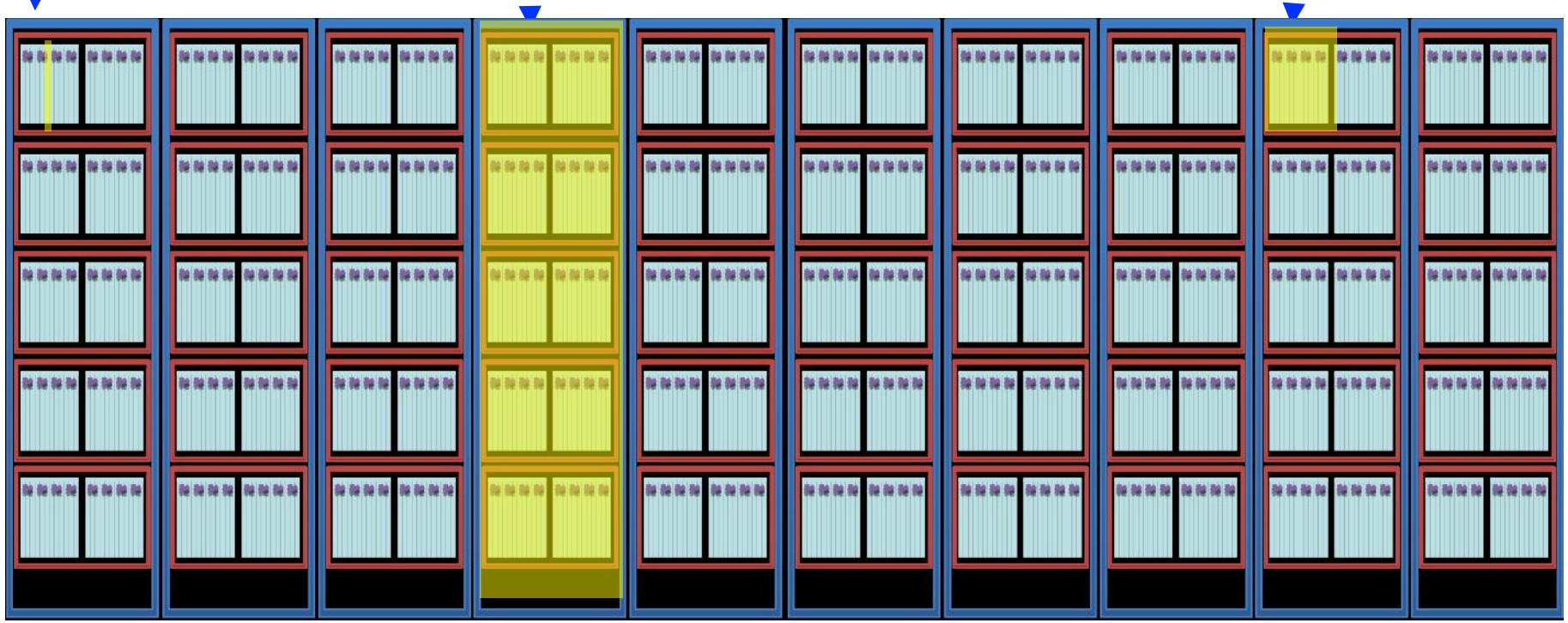
SpiNNaker machines

103 machine: 864 cores, 1 PCB, 75W

104 machine:10,368 cores, 1 rack, 900W
(NB 12 PCBs for operation without aircon)

105 machine: 103,680 cores, 1 cabinet, 9kW



106 machine: 1M cores, 10 cabinets, 90kW

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The networking challenge

- Emulate the very high connectivity of real neurons
- A spike generated by a neuron firing must be conveyed efficiently to >1,000 inputs
- On-chip and inter-chip spike communication should use the same delivery mechanism

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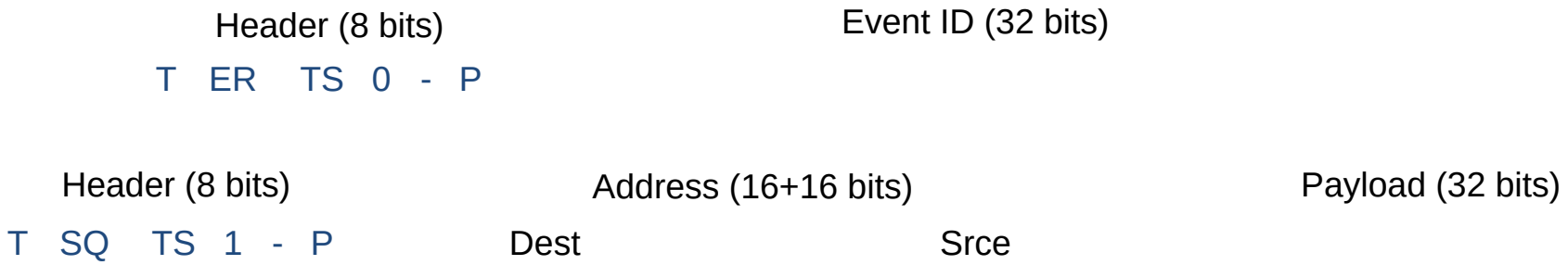
Network – packets

- Four packet types
  - MC (multicast): source routed; carry events (spikes)
  - P2P (point-to-point): used for bootstrap, debug, monitoring, etc
  - NN (nearest neighbour): build address map, flood-fill code
  - FR (fixed route): carry 64-bit debug data to host
- Timestamp mechanism removes errant packets
  - which could otherwise circulate forever



Network – MC Router

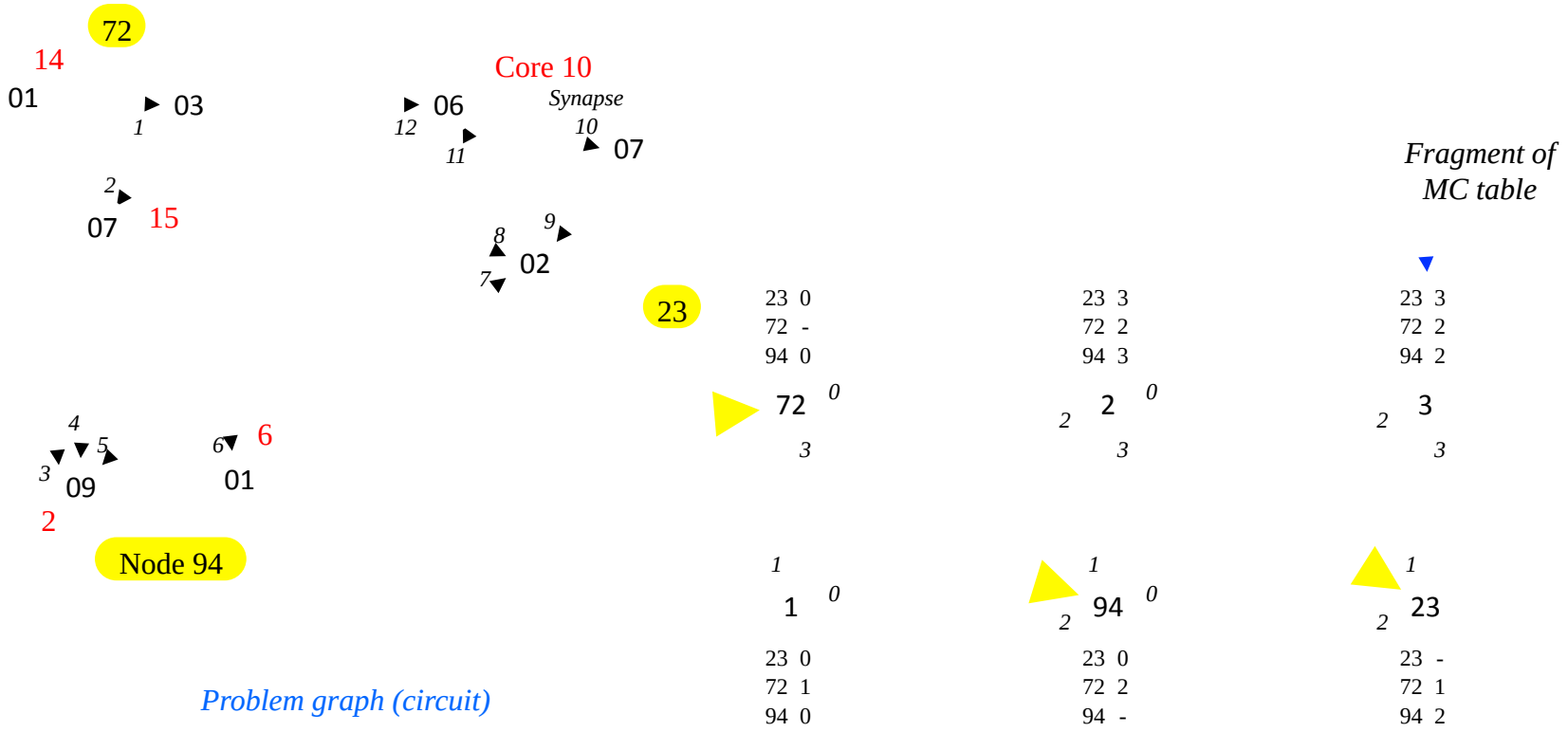
- All MC spike event packets are sent to a router
- Ternary CAM keeps router size manageable at 1024 entries (but careful network mapping also essential)
- CAM 'hit' yields a set of destinations for this spike event
  - automatic multicasting
- CAM 'miss' routes event to a 'default' output link

Event ID

0 0 1 0 X 1 0 1 X ▸ 0000000100000100000 001001

On-chip Inter-chip

Topology mapping



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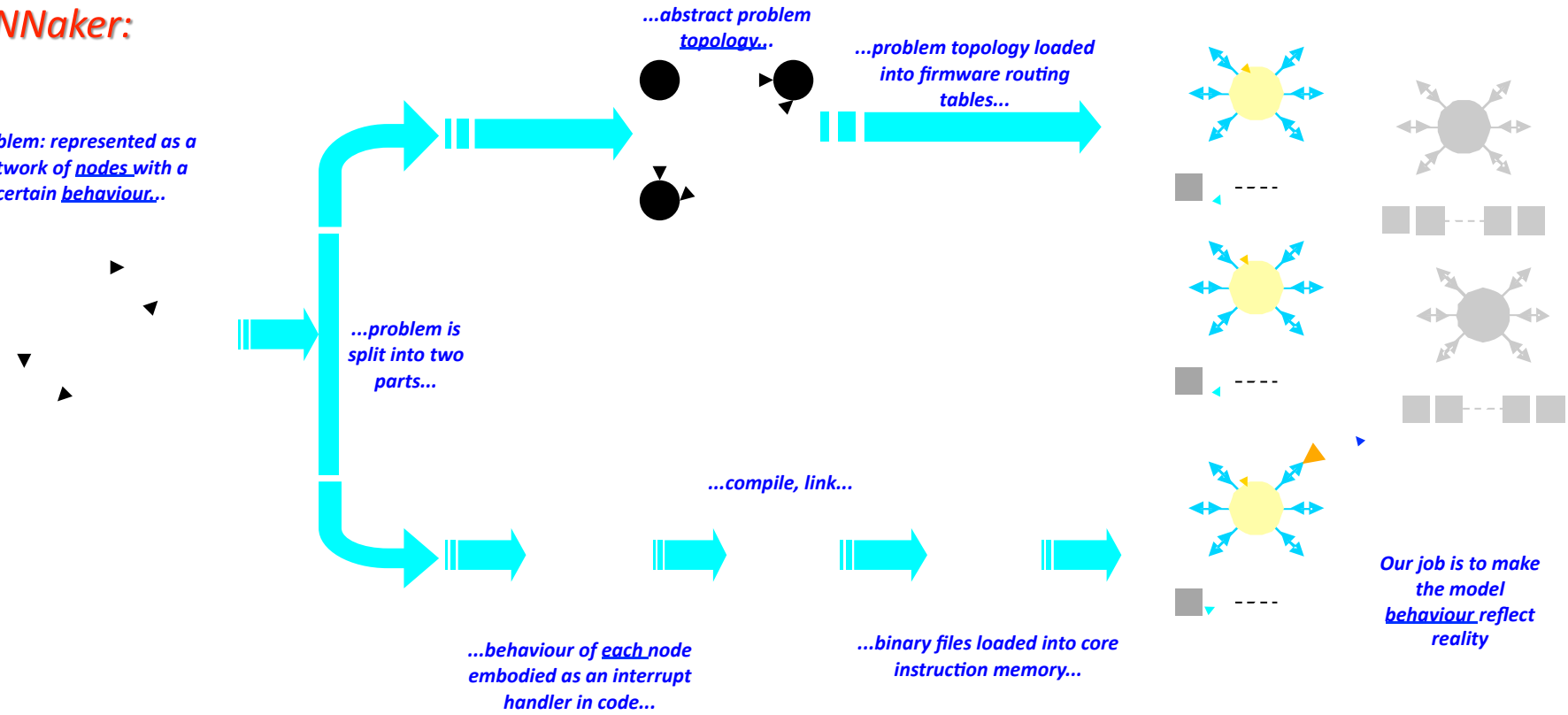
Problem mapping

SpiNNaker:



The code says "send message" but has no control where the output message goes

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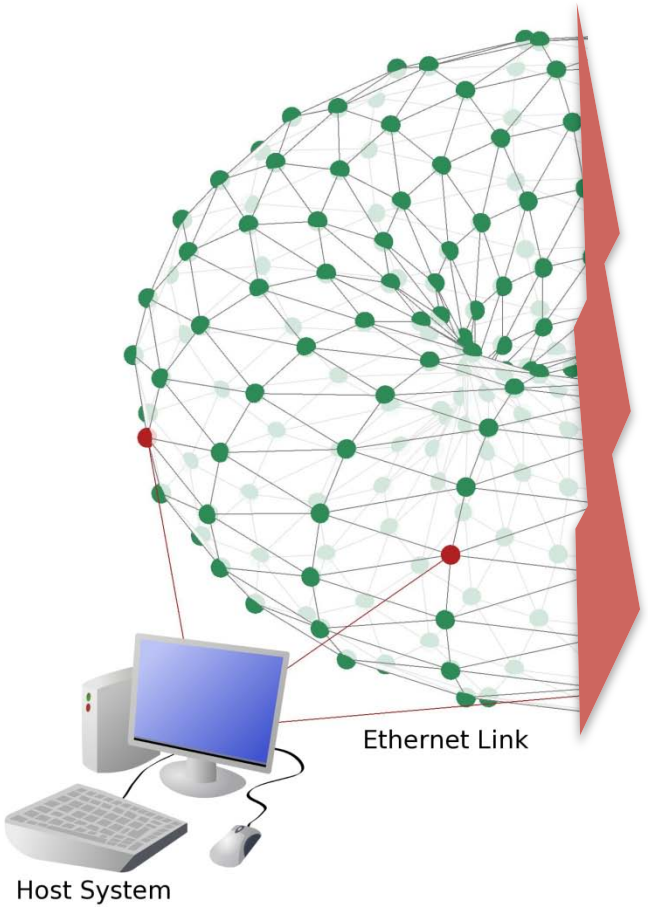
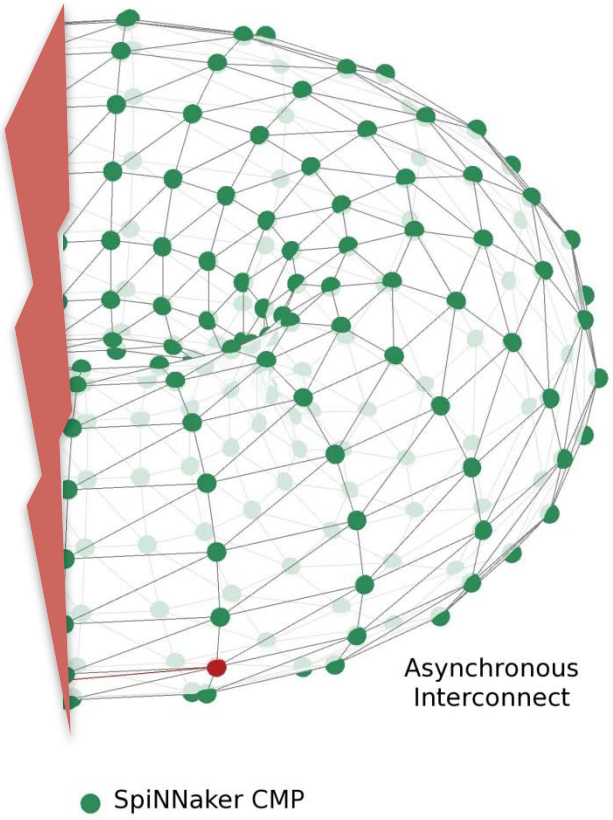
Bisection performance



- 1,024 links
  - in each direction
- ~10 billion packets/s
- 10Hz mean firing rate
- 250 Gbps bisection bandwidth



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Partially-Ordered Event-Driven Systems

- A set of dynamical processes $P = \{P_i\}$
  - $S_i(t)$ is the state of P_i at time t
- A set of event channels $E = \{E_j\}$
  - E_j carries a time series of asynchronous impulses
  - generated by a process $E_j = e_j(P_j)$
- Hybrid model (biology): processes evolve $S_i = s_i(t, E^* \subseteq E)$
- Discrete model (*SpiNNaker*)
  - time can be abstracted into a series of (e.g.) 1ms events E_t
  - We can model each event atomically: $E_j \Rightarrow S_i := p_i(S_i, j)$
- In practice, on *SpiNNaker* event handling takes a finite time and may overlap subsequent events.

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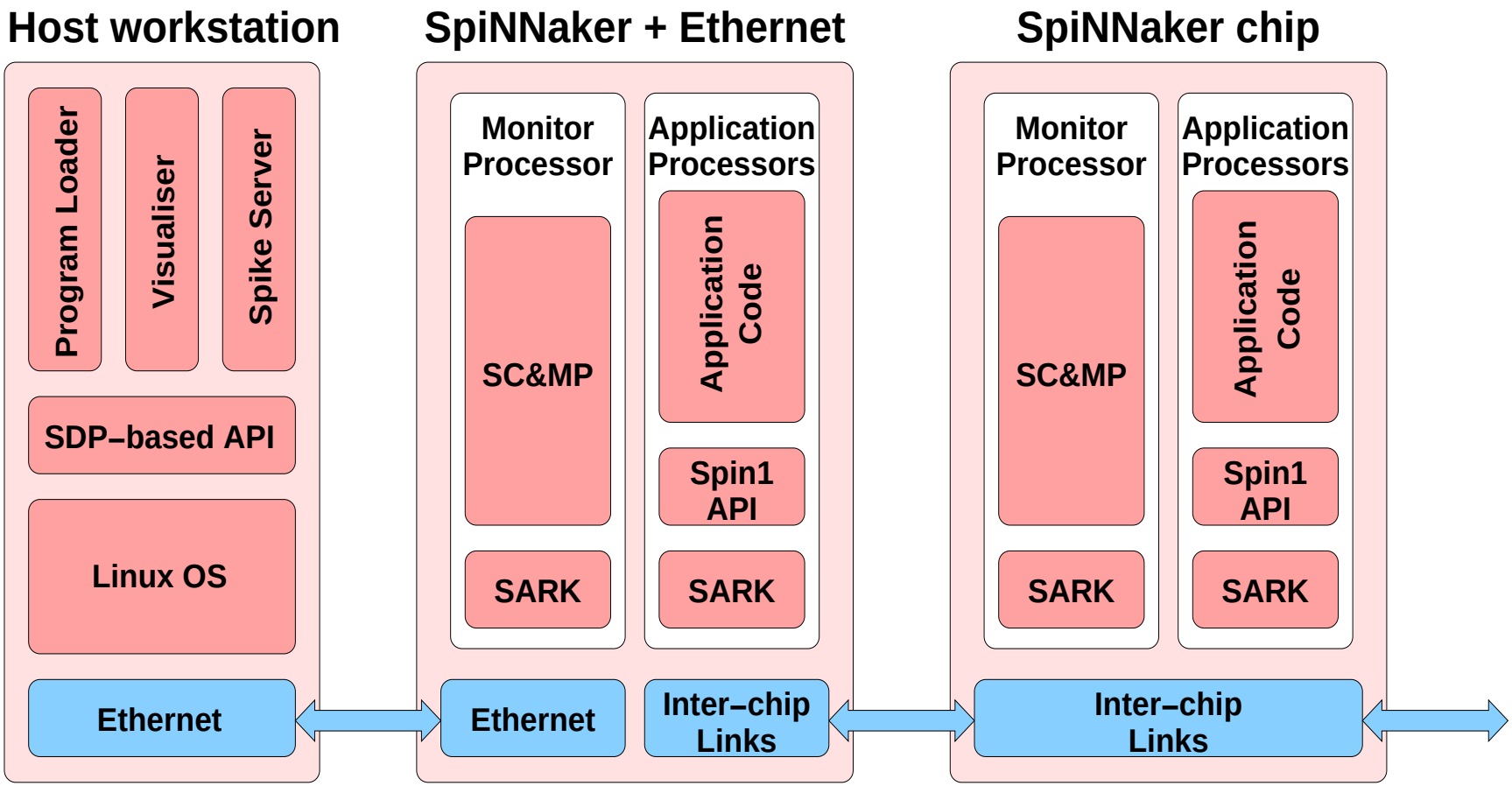
Software overview



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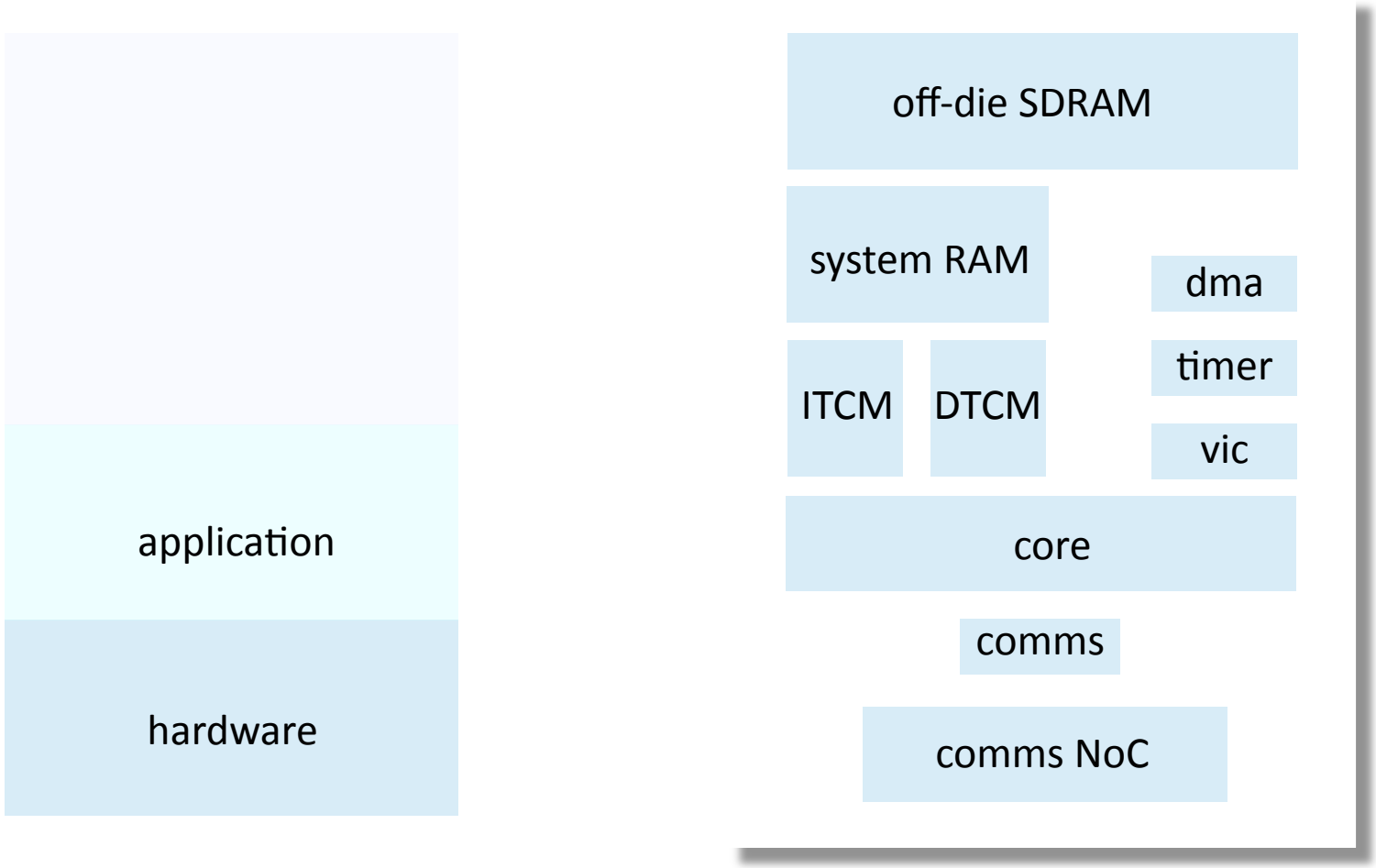
Hardware resources



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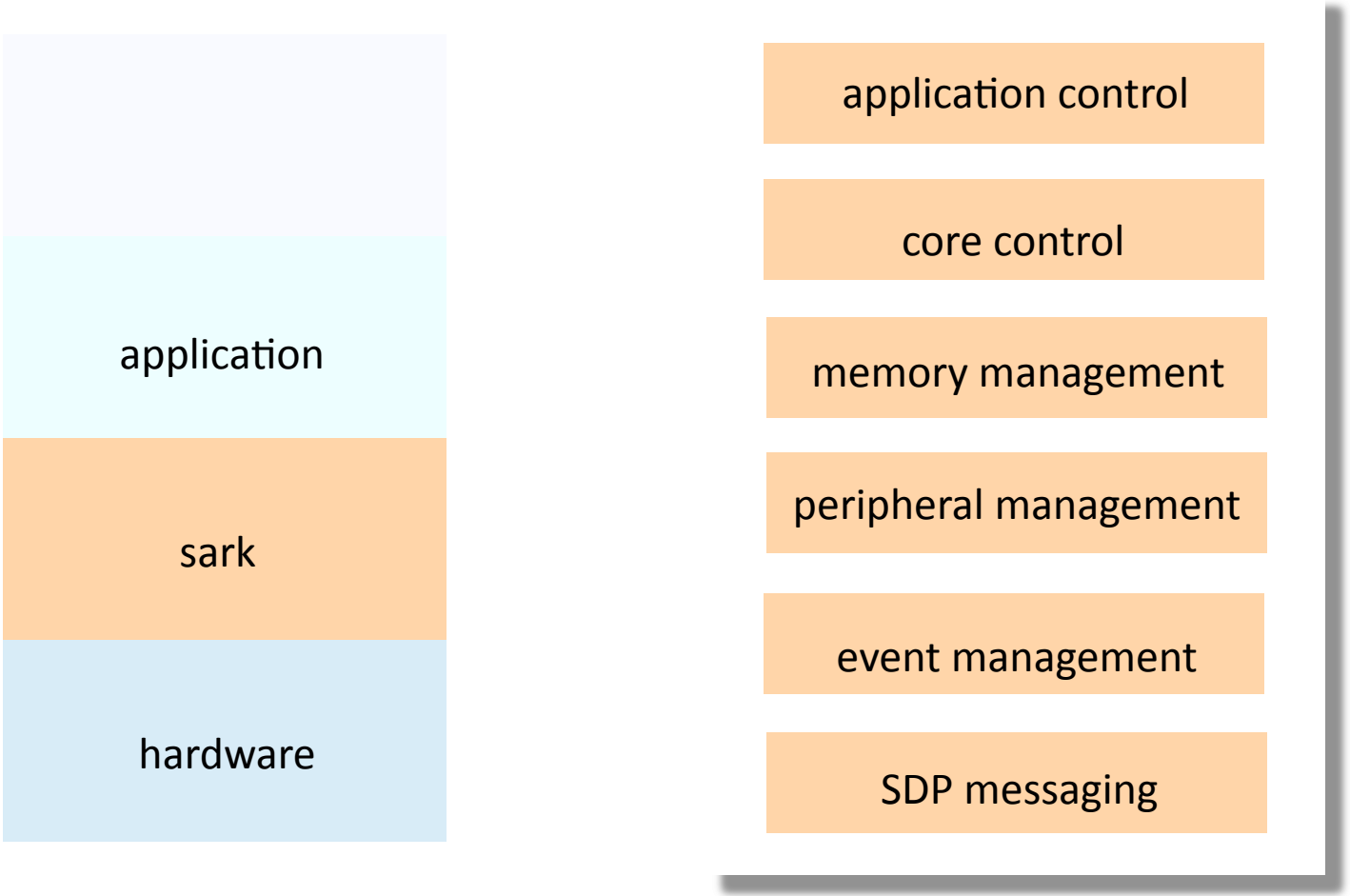
SARK: low-level software



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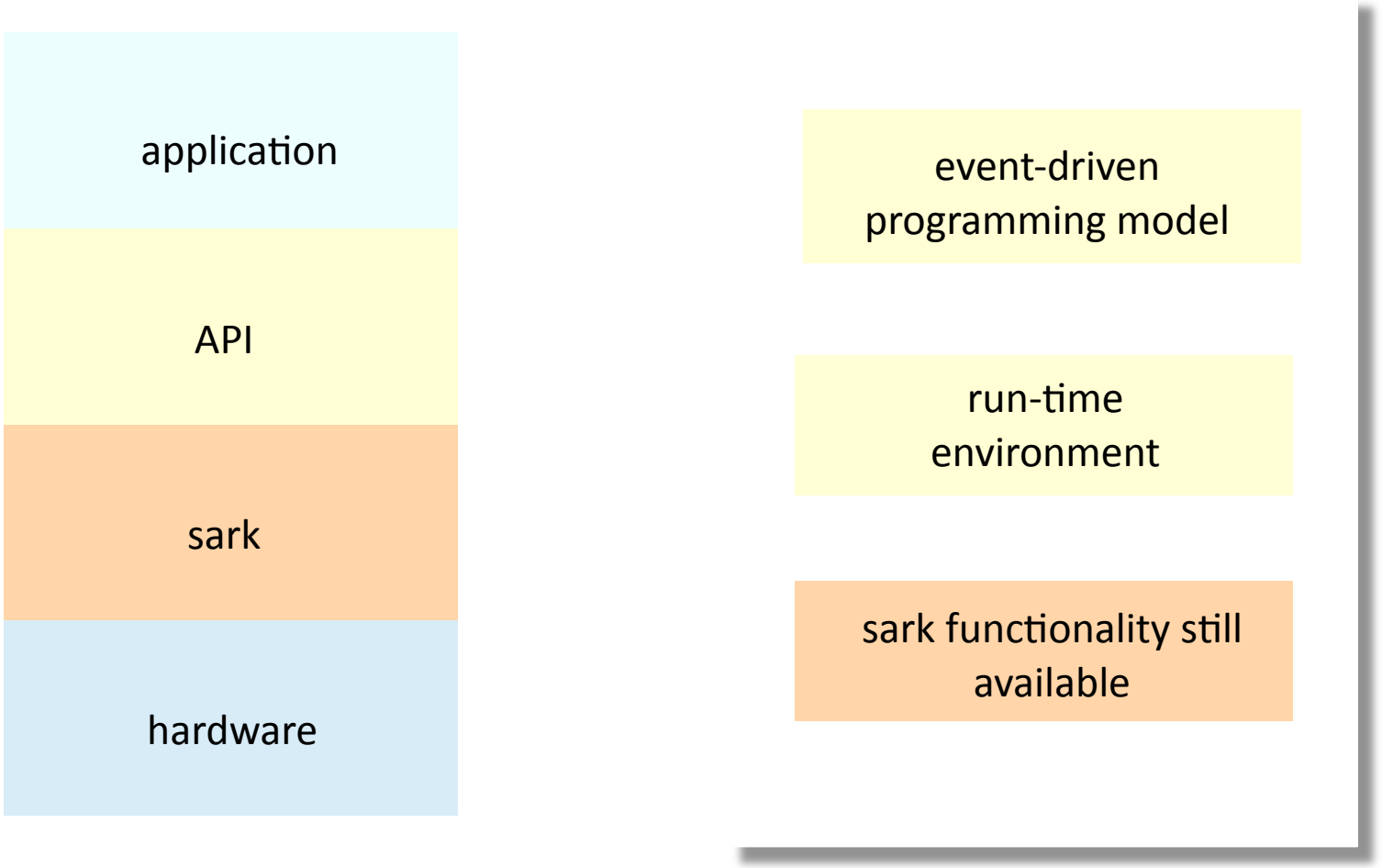
API: run-time environment



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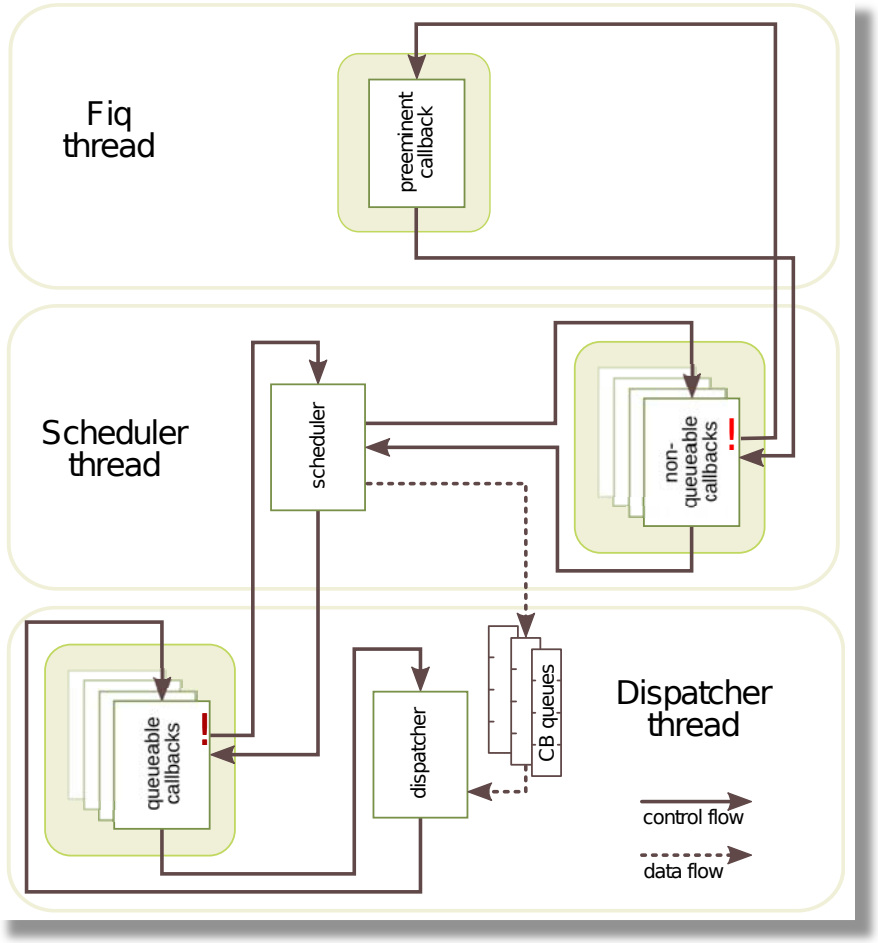
Priorities

priority level = -1
only one callback
cannot be pre-empted

priority level = 0
can only be pre-empted
by priority -1 callback

priority level > 0
can be pre-empted
by priority <= 0 callbacks
scheduled in priority order



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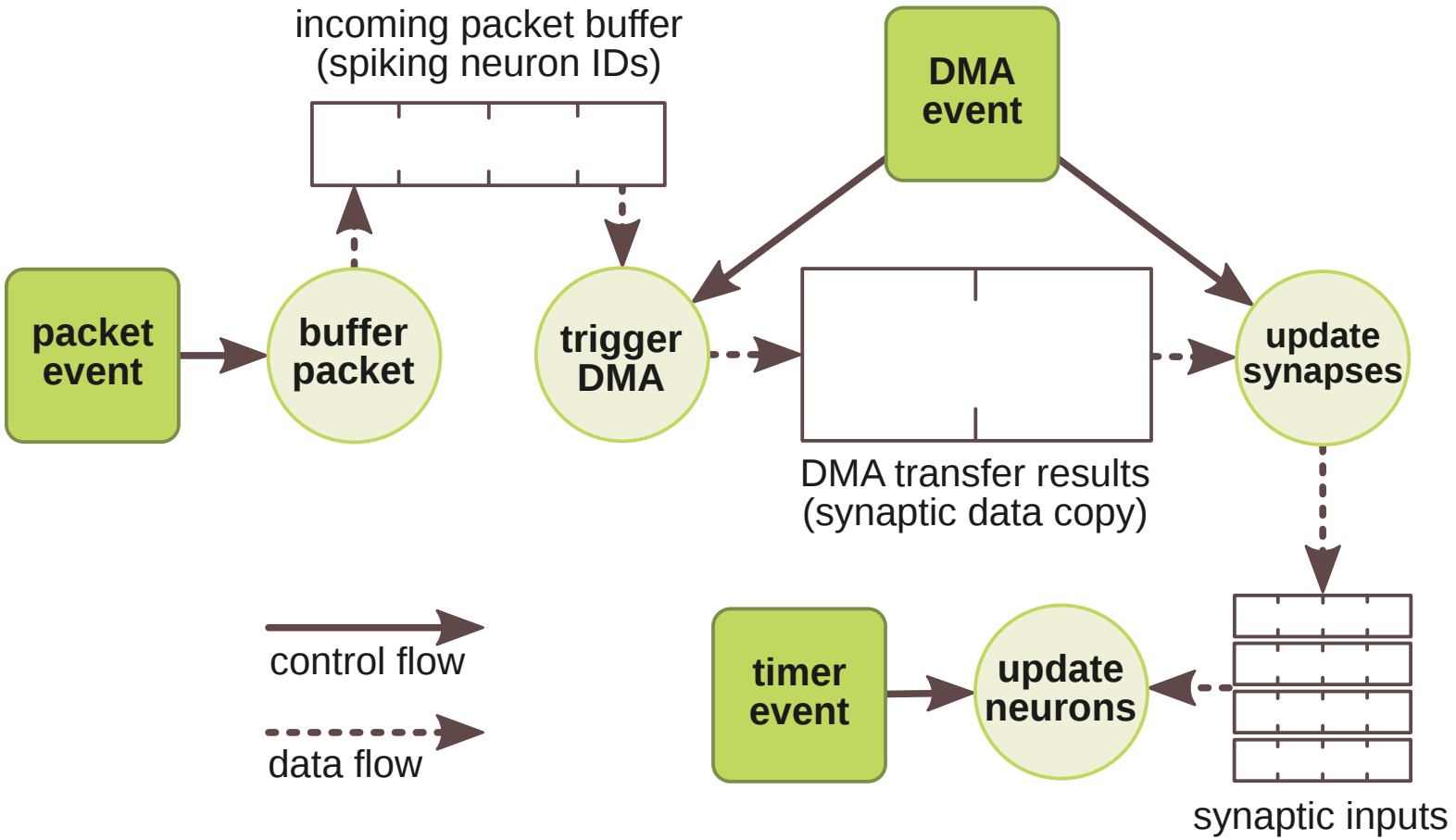
Event-driven software model



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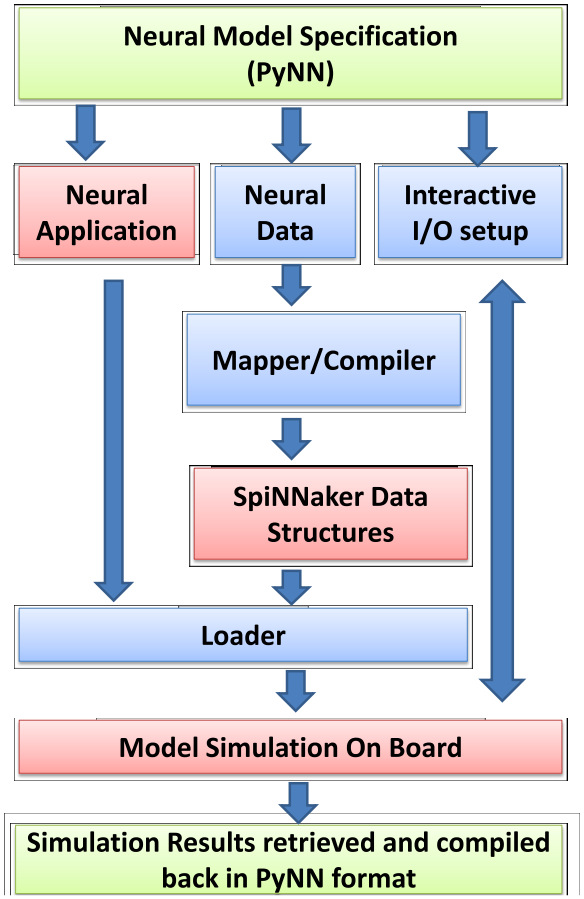
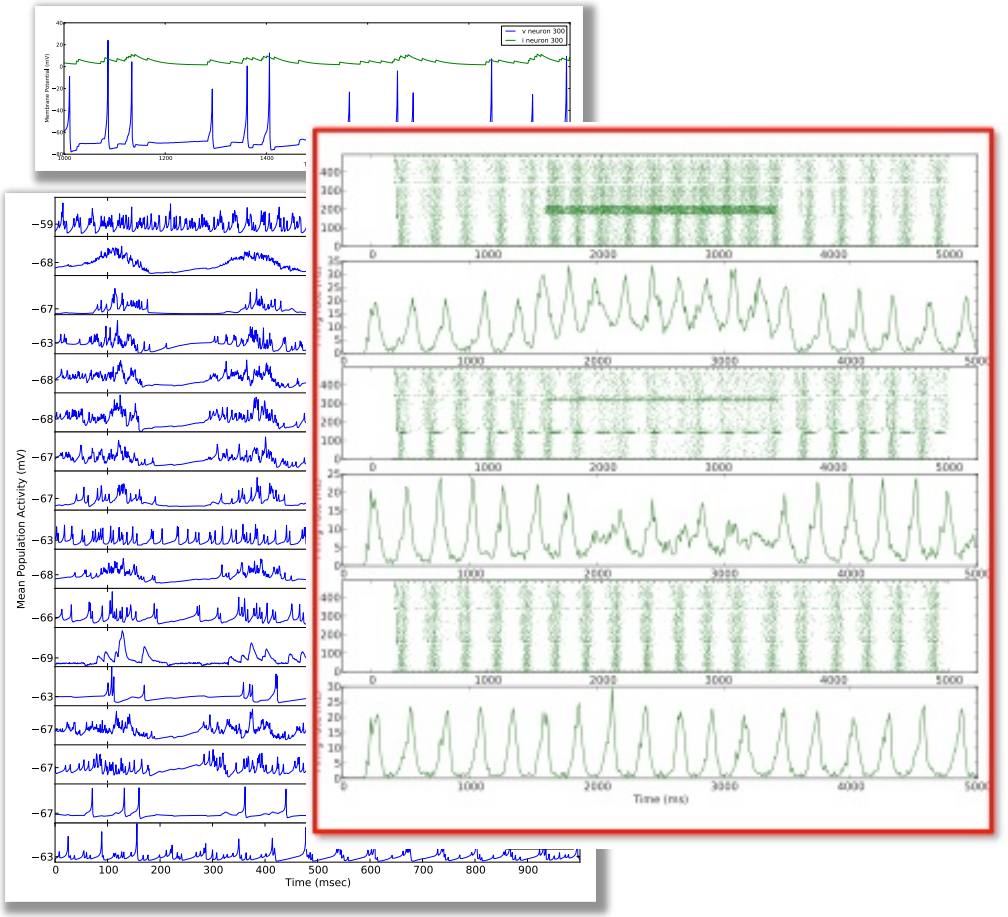
PyNN design flow





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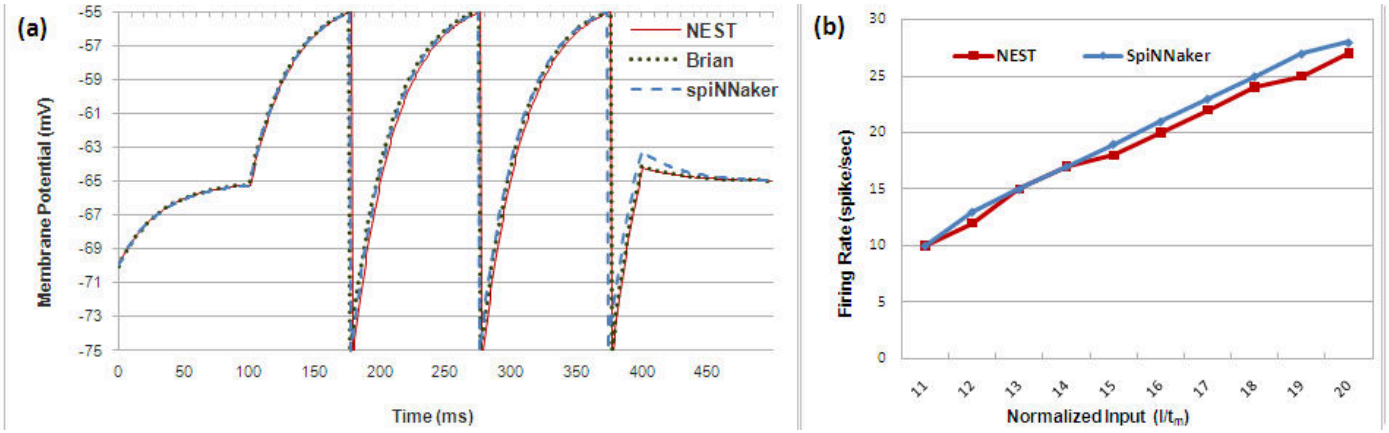
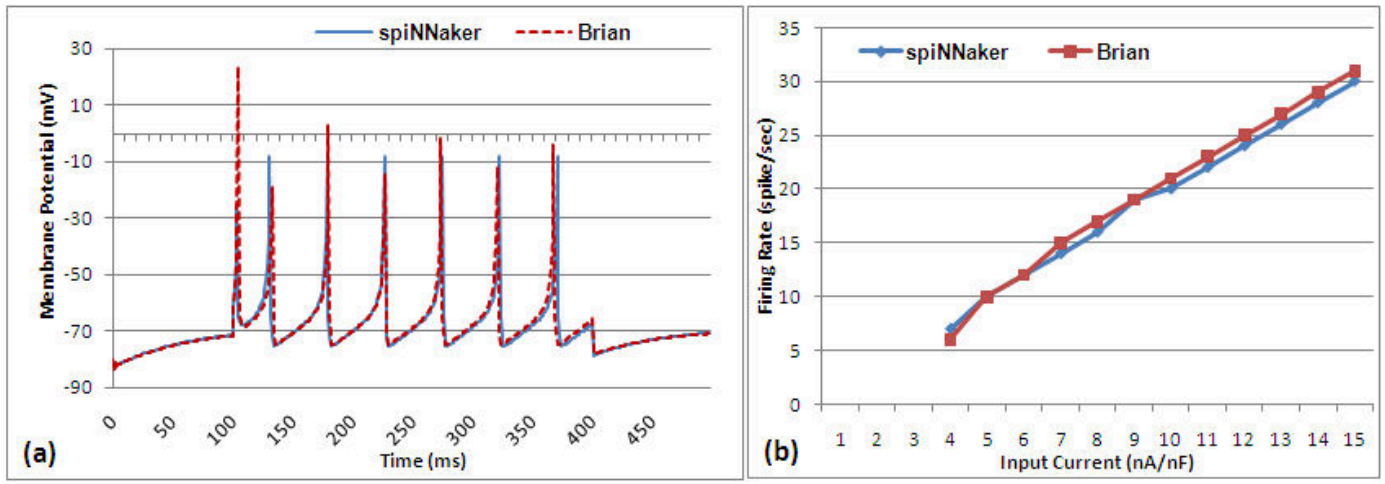
PyNN integration

- LIF



- Izhikevich



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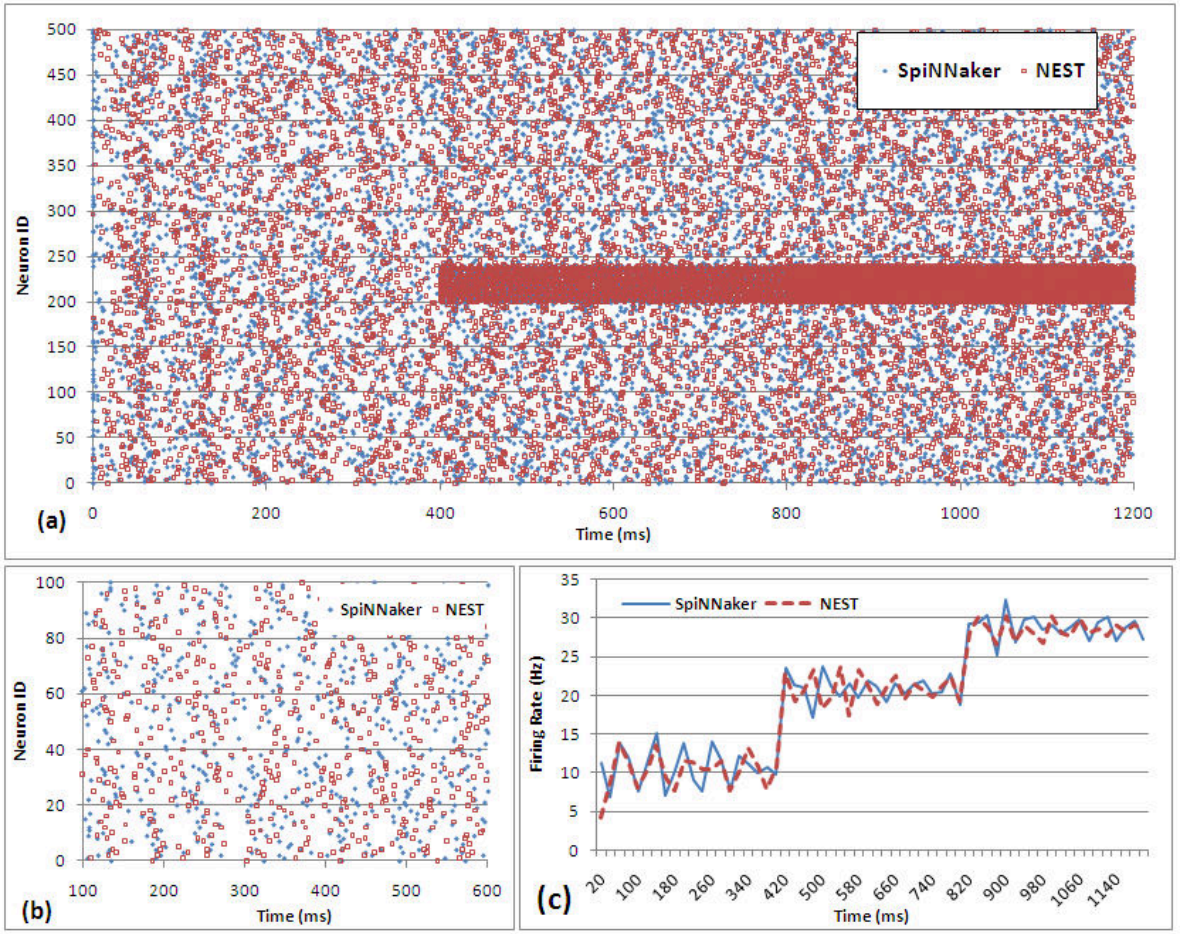
PyNN integration

- Vogels-Abbott benchmark
  - 500 LIF neurons



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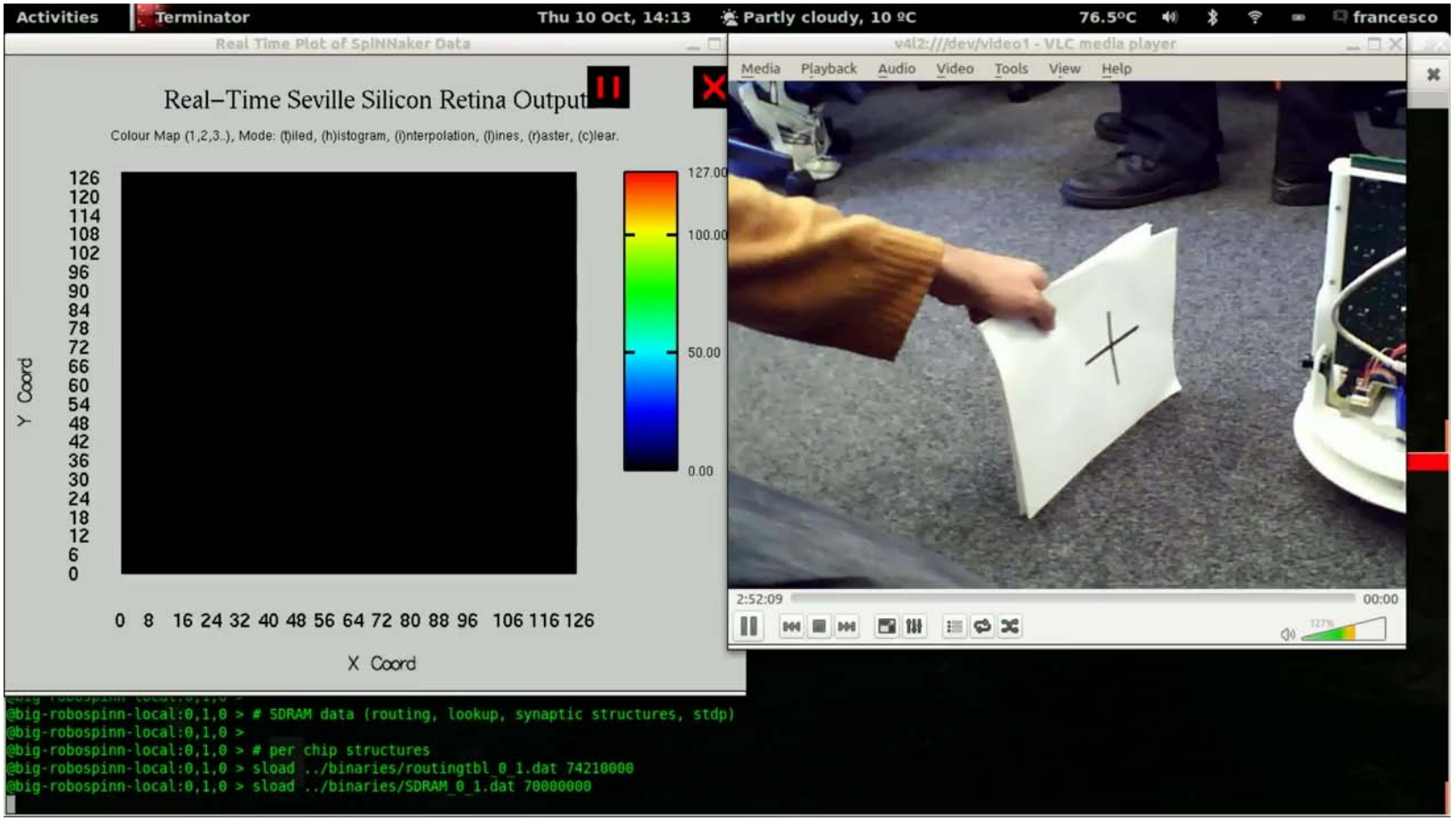
SpiNNaker robot control



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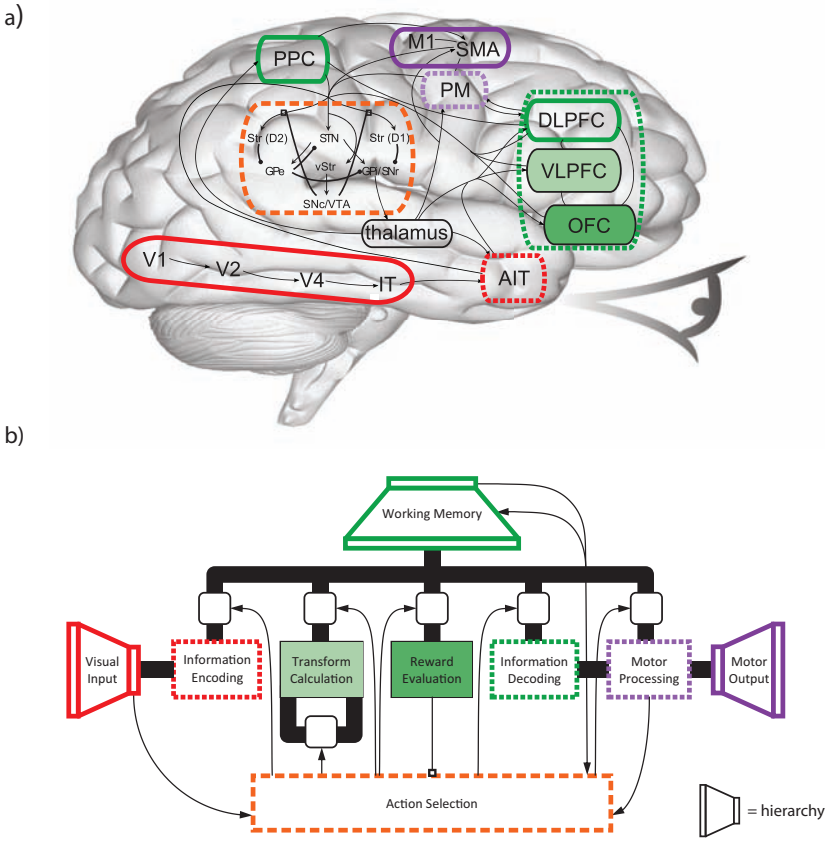
Spaun

- SpiNNaker:
  - 5M conn/s/ARM
- Spaun:
  - 2.5M neurons
  - ~100Hz firing rates
  - ~500 inputs/neuron
  - 125G conn/s
- Real-time Spaun:
  - 25,000 ARMs
  - 30x 48-node PCB
  - by end 2013?



Chris Eliasmith et al, Science vol. 338, 30 Nov 2012

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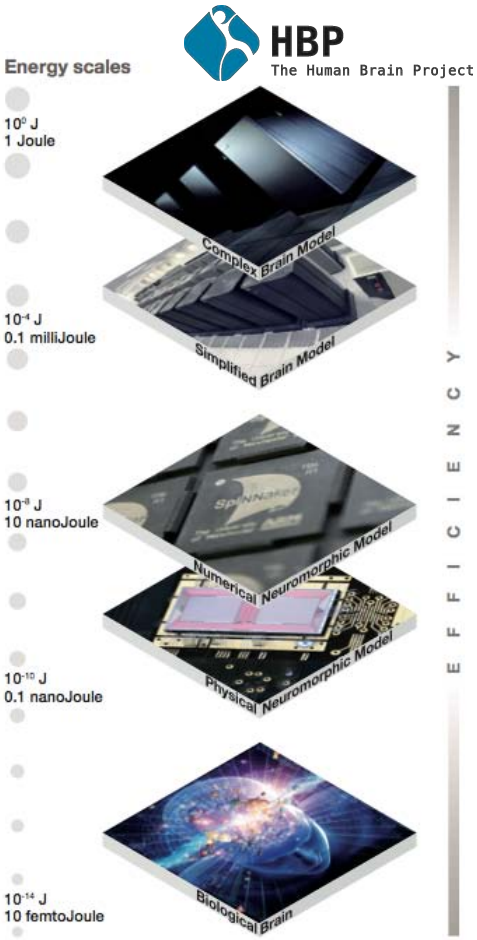
Conclusions

- Brains represent a significant computational challenge
  - now coming within range?
- *SpiNNaker* is driven by the brain modelling objective
  - virtualised topology, bounded asynchrony, energy frugality
- The major architectural innovation is the multicast communications infrastructure
- We have working hardware & software
  - 48-node 864-ARM PCBs now
  - first multi-PCB systems now working



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